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150045-DV

# The United States of America



## The Commissioner of Patents and Trademarks

*Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.*

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## United States Patent

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*T. Todd Johnson*

Commissioner of Patents and Trademarks

*Allie M. Person*

Attest



US005903260A

## United States Patent [19]

Imamura

[11] Patent Number: 5,903,260

[45] Date of Patent: May 11, 1999

[54] FLAT PANEL DEVICE AND DISPLAY DRIVER  
WITH ON/OFF POWER CONTROLLER  
USED TO PREVENT DAMAGE TO THE LCD

[75] Inventor: Youichi Imamura, Suwa, Japan

[73] Assignee: Seiko Epson Corporation, Tokyo,  
Japan

[21] Appl. No.: 08/582,771

[22] Filed: Jan. 2, 1996

## Related U.S. Application Data

[62] Division of application No. 08/267,103, Jun. 23, 1994, Pat. No. 5,563,624, which is a continuation of application No. 07/834,295, Apr. 9, 1992, abandoned, filed as application No. PCT/JP91/00785, Jun. 11, 1991.

## [30] Foreign Application Priority Data

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Jun. 11, 1991 [WO] WIPO ..... PCT/JP91/00785

[51] Int. Cl.<sup>6</sup> ..... G09G 5/00; G05B 11/01

[52] U.S. Cl. .... 345/211; 364/141

[58] Field of Search ..... 345/87, 98, 99,  
345/100, 117, 204, 205, 206, 211, 212,  
213; 315/169.4; 363/86; 340/825.5; 395/750.01,  
750.04, 750.07, 700.08; 364/140, 141, 142,  
143, 144

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Primary Examiner—Jeffery Brier

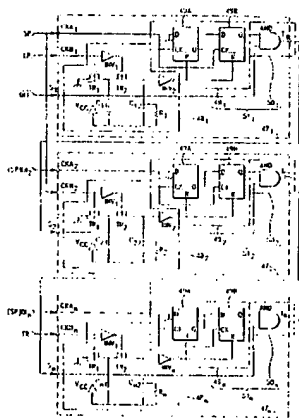
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## [57] ABSTRACT

Signal management control units 47<sub>1</sub>–47<sub>n</sub> of respective scan drivers LSI in an LCD module are cascade-connected and each have the same construction. A detected signal of the signal management control unit 47<sub>1</sub> is a data signal latch clock LP applied to a terminal CKB<sub>1</sub>. A detected signal of the signal management control unit 47<sub>2</sub> is a frame start signal SP applied to a terminal CKB<sub>2</sub>. A detected signal of the signal management control unit 47<sub>n</sub> is an AC-transforming clock FR applied to a terminal CKB<sub>n</sub>. The signal management control unit 47<sub>1</sub> includes a signal stop detection circuit 48 serving as a signal detection means for detecting a stop of the detected signal and a sequence processing circuit 51 consisting of a signal delay circuit 49 and a logic circuit 50. When stopping oscillations of, e. g., the frame start signal SP, outputs T<sub>1</sub>–T<sub>n</sub> of the circuit 51 change to an L level. Hence, a display-off signal DF of the LCD module assumes the L level. A liquid crystal panel is forcibly set in a display-off mode. As a result, even if the frame start signal SP is stopped due to some cause, a liquid crystal application voltage is set down to zero. It is, therefore, possible to avoid a liquid crystal DC drive and prevent a deterioration of the liquid crystal.

6 Claims, 9 Drawing Sheets



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